Dynamic Response of Jospephson Resistive Logic (RCJL) GATE

K.Srinivas and J. C. Biswas

ABSTRACT----In this paper a thorough investigation of resistive logic RCJL gate has been made. The current equations of this gate at each stage have been deduced. The dynamic response of this gate has been obtained by the computer-simulation. Our concept of turn-on delay has been introduced. The effect of overdrive current on turn-on delay for resistive logic gate has been shown. This will provide a better understanding of switching dynamics of the RCJL logic gate. Further, we have shown the effect of overdrive current on this logic gate.

1. INTRODUCTION

Two attractive features of SQUID devices for logic applications are isolation and serially connected fan-out. The isolation is provided by the transformer coupling between the SQUID and the input. The isolation is not perfect in the sense that a noise pulse (typically 5 percent) is fed back into the control line when the SQUID switches to the non-zero voltage. The other advantage is the serial fan-out capability by which the control lines of many load devices can be connected in series with a single output line.

The main drawbacks of SQUID devices for logic application are relatively large device area and high sensitivity to stray magnetic fields. In SQUID 80% of the area is occupied by the transformer [1]. Further, the high sensitivity to stray magnetic field requires that the SQUID based logic circuits be well shielded from the stray magnetic fields.

The resistive logic gates such as JAWS (Josephson Auto-Weber System) [2], DCI (Direct Coupled Isolation) [3] and RCJL (Resistor Coupled Josephson Logic) [4] are chosen because the gate logic delay in this case would consist of the turn-on delay, switching delay and propagation delay, but not the crossing delay as in the case of magnetically coupled logic gates. Further, these resistive logic gates do not have a factor of limiting the size very seriously. So, the gate propagation delay can be made sufficiently small. Therefore, the small time constant of the Josephson junction can be directly attained to these gates.

It has been considered by the earlier workers [5] that the turn-on delay of a logic gate is the time taken for the logic gate to obtain 2% of the output current to the load. This consideration seems to be arbitrary.

Due to this fact, in the present paper we have made a thorough investigation of the resistive logic gates. Our concept of turn-on delay [6] has been introduced which will be able to remove the confusion in critically ascertaining the switching speed of these logic gates. Further, the effect of overdrive current on these resistive logic gates has been studied.

1. DEPARTMWENT OF PHYSICS, GMR INSTITUTE OF TECHNOLOGY, RAJAM-532127,A.P., INDIA Email : srinkura@gmail.com srinivas.k@gmrit.org
2. DEPARTMENT OF ELECTRONICS AND ELECTRICAL COMMUNICATION ENGINEERING, INDIAN INSTITUTE OF TECHNOLOGY , KHARAGPUR-721302 INDIA.

2. RCJL (Resistor Coupled Josephson Logic)

The curcuit configuration and the threshold curve for the RCJL gate are shown in Fig.l. The junctions J1, J2 and J3 have critical currents Io, 3/2 Io, and 3/2 Io, and junction capacitances of Cj, 3/2 Cj, and 3/2 Cj, respectively. The resistor R2, R3 and R4 have the same values of the resistance r' and the resistance of R1 is r. The RCJL gate is biased in the superconducting state by the injection of the input current Iin. The junction J2 plays a role of the current-summing junction in this gate. The operation of the RCJL gate is as follows:

Intially the gate current Ig splits into Igl and I g2 in the inverse ratio of resistors r2 and r3. When the input current Iin (Ic) is applied at the node C, the Iin goes through the junction J1 and is injected into the junction J2. The junction J2 subsequently switches from the superconducting state to the resistive state. A fraction of the Josephson current having shown in J2, swings over the junction J3 through r2, r3, r4, and causes J3 to switch. Consequently, the gate current Ig is steered towards the junction J1, and J1 switching results. After J1 switching, Ig is steered into the load Rl and I in is teriminated through Rl. Gate switching with input-output isolation is completed. In the RCJL gate, total Iin current contributes to initialization of the switching sequence, while only a fraction of Ig contributes to it. This results in a high input sensitivity.

According to Fig.2, the current equations at each statge of the RCJL gate can be written as:

$I_g = i_3 + i_4 + i_5 + i_6$ ---- (1)

$I_{in} + i_5 = i_7$ ---- (2)

$$i_3 = \frac{3}{2} I_0 \sin\theta_b + \frac{3}{2} C_j \frac{\phi_o}{2\pi} \frac{d^2\theta_b}{dt^2} \text{ --- (3)}$$

$$i_4 = \frac{3}{2} I_0 \sin\theta_a + \frac{3}{2} C_j \frac{\phi_o}{2\pi} \frac{d^2\theta_a}{dt^2} \text{ ---- (4)}$$

$$i_5 = I_0 \sin(\theta_a - \theta_c) + C_j \frac{\phi_o}{2\pi} \frac{d^2}{dt^2}(\theta_a - \theta_c) \quad \text{- (5)}$$

$I_6 = Vb/RL$ ----(6)

$I_7 = Vc/R1$ ----(7)

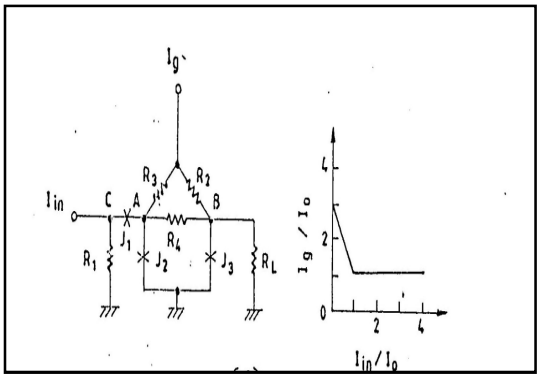


Fig. 1 Circuit configuration of the resistive logic RCJL gate with threshold characteristics.

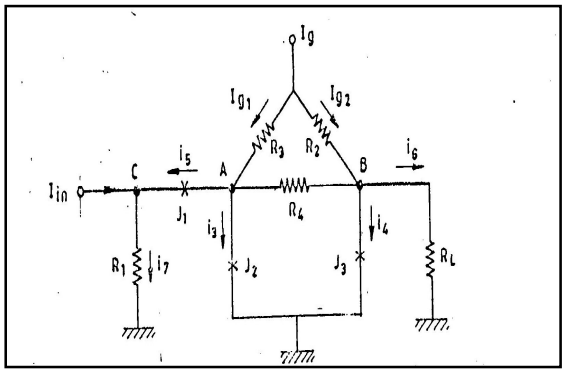


Fig. 2 Circuit configuration of the resistive logic RCJL gate with current indication at each stage of the logic gate

For Static case

At t = 0, Va = Vb = Vc = 0 =>

$$\frac{d\theta_a}{dt} = \frac{d\theta_b}{dt} = \frac{d\theta_x}{dt} = 0$$

Substituting the above conditions in Eqns. (1) and (2), we get

$$\frac{I_g}{I_0} = \frac{3}{2}(\sin\theta_a + \sin\theta_b) - \frac{I_{in}}{I_0} \quad \text{-----(I)}$$

Egn.(I) describes the static behaviour of the RCJL gate. A static curve between Ig/10 and Iin/I0 will give the operating margin and gain margins of the RCJL gate.

(b) Dynamic case:

Egn.(1) can be written as

$$Ig = I_0 \sin(\theta_a - \theta_c) + \frac{3}{2} I_0 (\sin\theta_a + \sin\theta_b) + Cj \frac{\phi_o}{2\pi} \frac{d^2}{dt^2}(\theta_a - \theta_c) + \frac{3}{2} C_j \frac{\phi_o}{2\pi}\left(\frac{d^2\theta_a}{dt^2} + \frac{d^2\theta_b}{dt^2}\right) + \frac{1}{r_L}\frac{\phi_o}{2\pi}\frac{d\theta_b}{dt} \quad \text{--- (8)}$$

$$\frac{\phi_o}{2\pi}\frac{d\theta c}{dt} = r\,(I_{in} + I_0 \sin(\theta_a - \theta_c) + C_j \frac{\phi_o}{2\pi}\frac{d^2}{dt^2}(\theta_a - \theta_c) \quad \text{--- (9)}$$

Also,

$$\frac{\phi_o}{2\pi}\left(\frac{d\theta_a}{dt} - \frac{d\theta_b}{dt}\right) = (I_0 \sin\theta_b + C_j \quad \text{--(10)}$$

$$\frac{\phi_o}{2\pi}\frac{d^2\theta_b}{dt^2} + \frac{2}{3}\frac{\phi_o}{2\pi r^L}\frac{d\theta_b}{dt} - \frac{I_g}{3})\, r^1$$

From Eqns. (8),(9) and (10) we can obtain the following expressions:

$$\frac{d^2\theta_a}{dt^2} = \frac{4\pi}{3\phi_o C_j}$$

$$(\frac{I_g}{2} + I_{in} - \frac{3}{2} I_0 \sin\theta_a \quad \text{------ (II)}$$

$$-\frac{\phi_o}{2\pi r}\frac{d\theta_c}{dt} - \frac{3\phi_o}{4\pi r^1}\frac{d}{dt}(\theta a - \theta b))$$

$$\frac{d^2\theta_b}{dt^2} = \frac{2\pi}{\phi_o C_j}(\frac{I_g}{3} + \frac{\phi_o}{2\pi r^1}\frac{d}{dt}(\theta_a - \theta_b) \quad \text{-- III)}$$

$$-I_0 \sin\theta_b - \frac{2}{3} - \frac{\phi_o}{2\pi r_L}\frac{d\theta_b}{dt}]$$

$$\frac{d^2\theta_c}{dt^2} = \frac{2\pi}{\phi_o C_j}\left(\frac{I_g}{3}+\frac{5}{3} I_{in}\right.$$

$$- I_0 \sin\theta_a + I_0 \sin(\theta_a - \theta_x)$$

$$\left. - \frac{5\phi_o}{6\pi\, r}\frac{d\theta c}{dt} - \frac{\phi_o}{2\pi\, r^1}\frac{d}{dt}(\theta_a - \theta_c)\right) \text{ ---- (IV)}$$

Computer-simulated pulse response of the RCJL gate can be obtained by solving the Eqns. (II),(III) and (IV) for an input current Iin applied as a step function at t=0 with amplitude 1.5 Ith. To solve these equations the initial conditions for $\theta_a(\theta_{ao})$ and $\theta_b(\theta_{bo})$ are to be known which can be deduced as follows:
At t = 0, from Eqns. (1) and (2).

$$I_g = \frac{3}{2} I_0 \ (\sin\theta_a + \sin\theta_b)$$

Since the resistances R_2 and R_3 are equal,

$$\sin\theta_{a0} = \sin\theta_{b0} = \frac{Ig}{3I_0}$$

$$or\ \theta_{a0} = \theta_{b0} = \sin^{-1}\left(\frac{Ig}{2I_0}\right)$$

Also, at t = 0 ; I in = 0 ==> $i_5 = 0$

==> $\sin(\theta_{a0} - \theta_{c0}) = 0$ ===> $\theta_{a0} = \theta_{ac}$

$$\theta_{a0} = \theta_{b0} = \theta_{c0} = \sin^{-1}\left(\frac{I_g}{3I_o}\right)$$

Therefore,

The current variations with time for a RCJL gate at each stage have been plotted in Fig.3 using computer simulation.

The solid curve shows the current variation with time at point 'A' (as shown in Fig.2) and the dotted curve shows the output current variation with time.

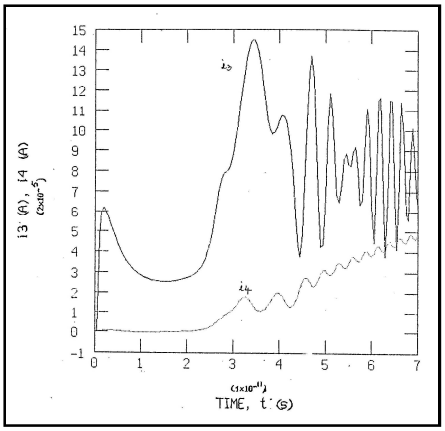
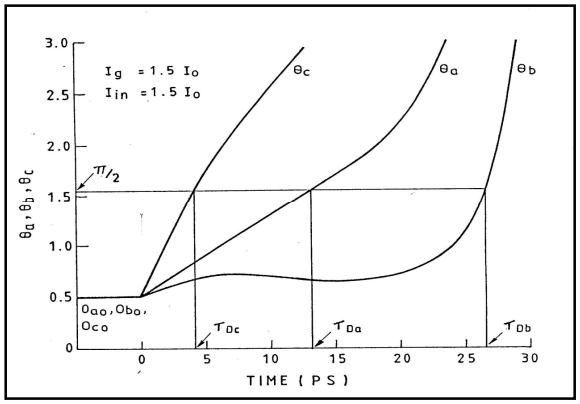


Fig.3 Simulated switching dynamics of the RCJL gate. Circuit parameters used in the simulation are from Nb/A10x/Nb Josephson technology and are given as Io = 0.087 mA, Cj = 0.37 pF, R1 = R2 = R3 = 0.8 Ω, rL = 10 Ω. The switching waveforms of currnet flowing in the input resistor R and the output current respectively.

In Fig.4 we have shown the phase variations with time at different stages of the RCJL gate using computer simulation. The biasing and overdrive current conditions are as follows: Ig = 1.510 and Iin 1.510.

Using our concept[6] of turn-on delay, the turn-on delay at each stage of the RCJL gate has-- been



indicated. This will give an exact physical understanding of switching dynamics of the RCJL logic gate.

Fig. 4 Simulated phase evolution vs time for a RCJL gate. θa θb and θ, are the phase variations at points ca', 'b' and 'c' respectively. Circuit parameters used in the simulation are I0 = 0.087 mA, Cj = 0.37 pF, R1 = R2 = R3 = 0.8 and rL = 10 Ω.

Further, we have plotted (in Fig.5a and Fig.5b) the effect of overdrive current on turn-on delay for different biasing conditions Ig = 0.75I0, 1.510 and 2.2510. In Fig.5a and Fig5b the curve (a) indicates the TD vatiation at 4A1 (as shown in Fig.6.2c). Curve (b) shows the TD variation with overdrive at point B1. And curve (c) shows the TD variation at point CI with the overdrive. It can be observed from Fig.5 the turn-on

delay decreases as the overdrive increases. Also, the turn-on delay decreases with the increase of biasing current and overdrive currents. So, by choosing proper biasing and overdrive current we can minimize the turn-on delay of the RCJL gate.

Finally in Fig.6 we have compared the effect of turn-on delay vs overdrive for JAWS[7], DCI [8] and RCJL gates under the same biasing condition, Ig = 1.510. It is observed for the low fan-out (here fan-out is one) the DCI logic gate seems to be a better choice for the logic circuit application because of its low turn-on delay and high-speed

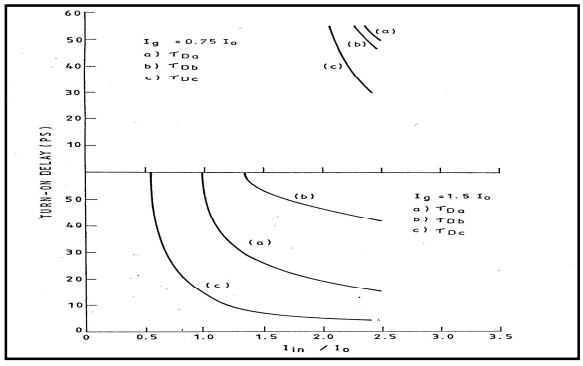


Fig. 5a Turn on delay of the RCJL gate vs input current. TDa' TDb and TDc represent the turnon delay variations with time at point 'a', 'b' and 'c' respectively (as shown in Fig. 2).

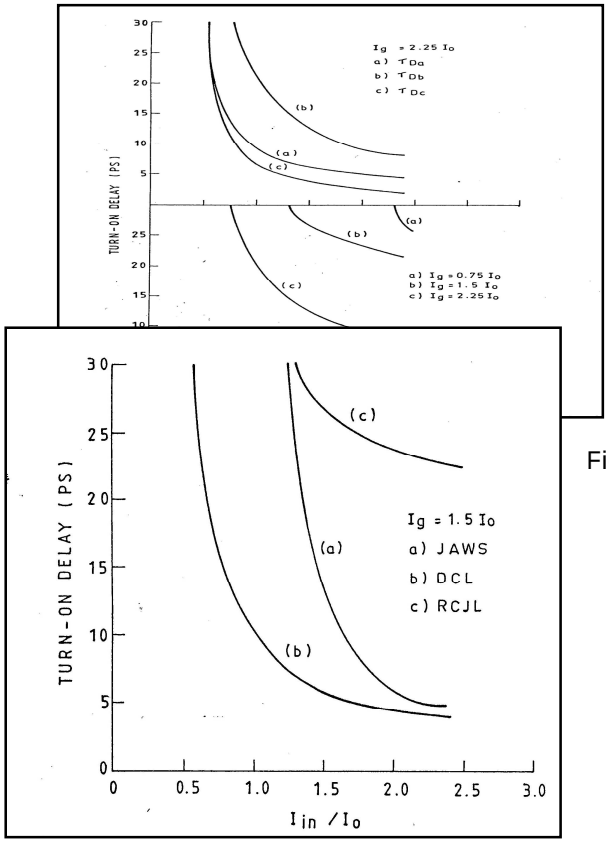


Fig. 5b Turn on delay of the RCJL gate vs input current. TDa' TDb and TDc represent the turnon delay variations with time at point 'a', 'b' and 'c' respectively (as shown in Fig. 2).

Fig. 6.14 Turn on delay vs input current of JAWS, DCI and RCJL gate under same biasing condition, Ig = 1.5I0.

3. CONCLUSIONS

A thorough investigation of RCJL logic gate has been made . The dynamic response of this logic gate is obtained by computer-simulation. The concept of our turn-on delay has been introduced which has helped us in critically ascertaining the switching speed of the logic gates. The effect of turn-on delay on overdrive current has been studied. It is observed that for low fan-outs, the DCI logic gate and for high fan-out RCJL gate seems to be a better choice for logic circuit application. It is expected that the concept of turn-on delay will be able to remove confusions which are lying in the earlier investigations.

REFERENCES

[1] T. R. Gheewala, " Josephson logic devices and circuits," IEEE Trans. Electron Devices vol.ED-27, no.10, October 1980, pp.1857-1869.

[2] T. A. Fulton, S. S. Pei and L. N. Dunkleberger, " A simple high performance current switched Josephson logic," Appl. Phys. Lett. . vol.34, no.10, May 1979, pp. 709-711.

[3] T. R. Gheewala and A. Mukherjee, " Josephson direct coupled logic (DCL)," IEDM Tech. Dig., (Washington DC, December 3-5, 1979), pp. 482-484.

[4] J. Sone, T. Yoshida and H. Abe, " Resistor coupled

Josephson logic," Appl. Phys. Lett. vol.40, 1982, p.741.

[5] J. Sone, " Turn-on delay analysis of current-injection Josephson circuits," J. Appl. Phys. vol.57, no.II, June 1985, pp. 5028-5034.

[6] K. Srinivas, J. C. Biswas , " Turn-on delay of a Josephson junction," J of Low

[7] Tempererature Physics" , vol.74, Nos. 5/6 1989 , pp.407-415.

[8] K. Srinivas, J. C. Biswas, " Dynamic response of Josephson resistive logic (JAWS) gate " , ICECS-11, INDONESIA (SUBMITTED)

[9] K. Srinivas, J. C. Biswas, " Dynamic response of Josephson resistive logic (DCI) gate " , ICASET-11, SINGAPORE (SUBMITTED)